ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

# Programmable $WSe_2$ 2D Lateral p-n Junctions Controlled by Dual Floating Gates

*Nuertai Jiazila, Peng Song, Chijun Wei, Xuanye Liu, Hui Gao, Jiequn Sun, Chengze Du, Hui Guo, Haitao Yang, Lihong Bao,* and Hong-Jun Gao*

**2D transition metal dichalcogenides (TMDs) materials with inherent flexibility, transparency, and sizable bandgap have gained significant attention as promising candidates for future semiconductor nanodevices. However, complementary doping in these 2D semiconductors remains a challenge because conventional ion implantation can lead to permanent damage to the atomically thin 2D channels. Here, programmable $WSe_2$ 2D lateral p-n homojunction controlled by dual floating gates on a $SiO_2$/Si substrate, achieving a rectification ratio of ≈$10^5$ and three dynamically switchable current levels is demonstrated. By injecting charges into two floating gates by applying voltage pulses with different polarities, lateral p-n, n-p, n-n, p-p homojunction can be formed. The ideality factors for the p-n and n-p junctions are extracted as ≈1.56 and ≈1.57, respectively. The $WSe_2$ p-n homojunction shows a maximum photovoltage responsivity of $6.67 \times 10^9$ V $W^{-1}$ under a weak light power of 0.09 nW. These results demonstrate outstanding electrical and optoelectronic properties in the programmable 2D lateral p-n junctions, establishing a solid foundation for the development of future non-volatile reconfigurable devices.**

## 1. Introduction

2D materials[1–3] have demonstrated superior electrical properties, stimulating both academic and industrial communities to devote significant efforts to explore these materials for their applications in field-effect transistors (FETs),[4–8] photodetectors,[9–12] light-emitting devices[11,13–15] and other electronic and photonic devices. One important aspect is that 2D materials could be used as an ultra-thin channel of an FET to immune short-channel effects and provide the opportunity for novel device concepts.[16,17] For electronics and microelectronics applications, developing 2D semiconductor doping methods is a key issue,[18] but the situation becomes unique when dealing with 2D materials. Due to the weak screening ability of the electric field in 2D materials, the defects created by high-energy particles during ion implantation form deep-level defects, acting as scattering centers to reduce mobility, and charge recombination centers to reduce carrier lifetime, thereby lowering the overall device performance.[19] Therefore, ion implantation doping techniques for 2D materials typically do not compromise their structural integrity and will introduce defect states into the energy band, degrading the device's performance.

As a basic device element, lateral p-n homojunctions based on 2D semiconductors have been achieved by adjusting the degree of energy band bending in the lateral direction of channel materials through methods such as split gates,[11,14,20–24] thickness engineering,[25,26] geometry-induced doping,[27–29] ferroelectric polarization,[30–33] semi-floating gates,[34–38] chemical doping,[39–42] surface charge transfer doping[43] and middle-floating gates.[44] However, charge density modulation via separate gates requires continuous external voltage input, making it difficult to achieve reconfigurable logic-in-memory functionality. Meanwhile, the gate-induced non-uniform charge distribution may reduce surface light emission.[45] Thickness engineering and surface charge transfer doping methods cannot be applied to industrial production and are unable to precisely modulate the energy band. In the case of ferroelectric-based modulation, non-volatility remains a key challenge, and the fatigue of ferroelectric materials has yet to be fully addressed.[46] Semi-floating gates, despite their good retention and endurance characteristics, cannot dynamically adjust the direction of lateral p-n junctions as flexibly as split gates. Chemical doping, while effective, is typically irreversible and may introduce defects and impurities; once completed, it is difficult to remove or adjust the doping levels through simple means. Therefore, developing a reliable, effective, and programmable doping method for construction of

N. Jiazila, P. Song, X. Liu, H. Gao, J. Sun, C. Du, H. Guo, H. Yang, L. Bao, H.-J. Gao
Beijing National Center for Condensed Matter Physics and Institute of Physics
Chinese Academy of Sciences
Beijing 100190, China
E-mail: lhbao@iphy.ac.cn

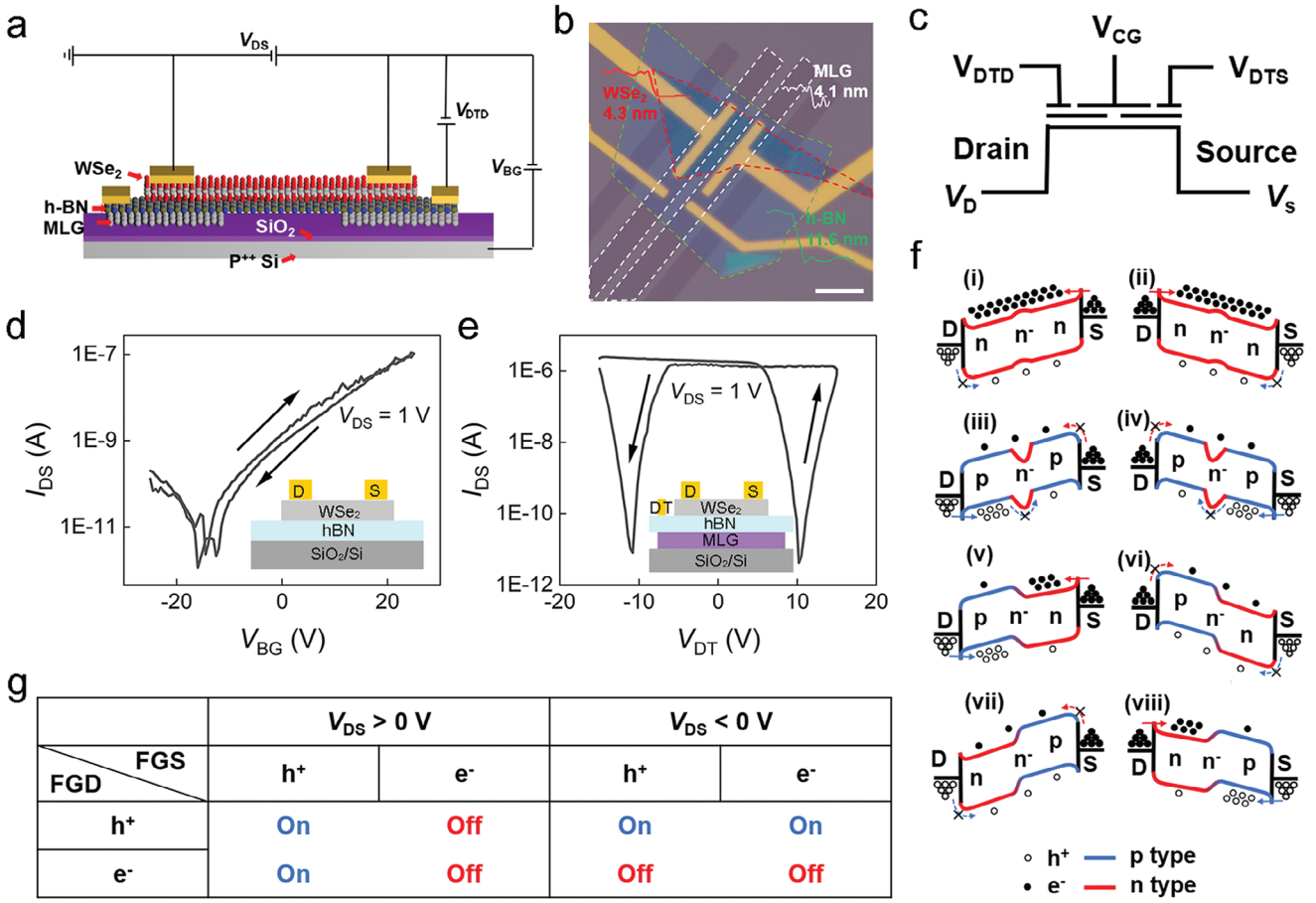
N. Jiazila, P. Song, C. Wei, X. Liu, H. Gao, J. Sun, C. Du, H. Guo, H. Yang, L. Bao, H.-J. Gao
School of Physical Sciences
University of Chinese Academy of Sciences
Beijing 100049, China

H. Guo, H. Yang, L. Bao, H.-J. Gao
Hefei National Laboratory
Hefei, Anhui 230088, China

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202423196

**DOI: 10.1002/adfm.202423196**




g

| FGD \ FGS | $V_{DS}$ > 0 V | | $V_{DS}$ < 0 V | |
|---|---|---|---|---|
| | h+ | e- | h+ | e- |
| h+ | On | Off | On | On |
| e- | On | Off | Off | Off |

**Figure 1.** Device architecture and energy band diagram of the $WSe_2$ lateral homojunction formed by dual floating gates modulation. a) Schematic of a $WSe_2$ lateral homojunction device. b) Optical image of a typical $WSe_2$ lateral homojunction device. The scale bar is 5 μm. c) The circuit diagram of a dual-floating-gate device. d) Dual-sweeping transfer curve of a $WSe_2$ FET with hBN-$SiO_2$ as the gate dielectric. The inset shows the device schematic diagram. e) Dual-sweeping transfer curve of a $WSe_2$ floating gate device. The inset shows the device schematic diagram. f) Energy band diagrams for different types of homojunctions under the given polarity of two floating gates. g) The different current states and majority carrier type in the device for the different polarity of floating gates (FGD and FGS) and $V_{DS}$.

lateral p-n homojunctions based on 2D semiconductors still remains a challenge. Zhe et al.[44] developed a middle-floating-gate field-effect transistor featuring specially shaped floating gates. By leveraging the controllable polarity through the interaction of the control gate, floating gate, and drain voltages, diverse current levels are achieved. This strategy of shaping floating gates offers several advantages, including high programming speed, reconfigurability, and enhanced memory performance.

In this work, we choose $WSe_2$, a typical bipolar 2D semiconductor with a bandgap of 1.65 eV,[47,48] as the channel materials with a vertically stacked $WSe_2$/hBN/multilayer graphene van der Waals heterostructure on a $SiO_2/p^{++}$ Si substrate to construct lateral p-n homojunctions programmed by dual floating gates (**Figure 1**). By applying voltage pulses to two direct tunneling electrodes with different polarities, charges can be stored/released in the two floating gates below the metal contact regions and different doping states of $WSe_2$ channel can be achieved, enabling the construction of lateral p-n, n-p, n-n, p-p homojunctions. For both p-n and n-p junctions, the rectification ratio can reach ≈$10^5$ and similar ideality factors (≈1.56 and ≈1.57, respectively) can be extracted. Moreover, the $WSe_2$ lateral homojunction exhibits typical photovoltaic functions, achieving a maximum electrical power conversion efficiency of 0.53%, a photovoltage responsivity of $6.67 \times 10^9$ V $W^{-1}$, and a peak external quantum efficiency of 2.4%. With its excellent electrical and optoelectronic characteristics, the device holds great potential for advancing future electronics and optoelectronics applications.

## 2. Results and Discussion

Figure 1a schematically shows the configuration of the $WSe_2$/hBN/graphene-based dual-floating gate field-effect transistor (DFG-FET) device, in which the $WSe_2$, hBN, MLG (multilayer graphene) act as the channel material, tunneling layer, floating gate, respectively. The two separating floating gates are aligned under the drain and source regions, respectively, to form a DFG-FET device. A typical DFG-FET device is shown in the optical image in Figure 1b. The device is fabricated by first exfoliating MLG on a $SiO_2/p^{++}$ Si substrate with a $SiO_2$ thickness of 285 nm, followed by stacking hBN and $WSe_2$ in

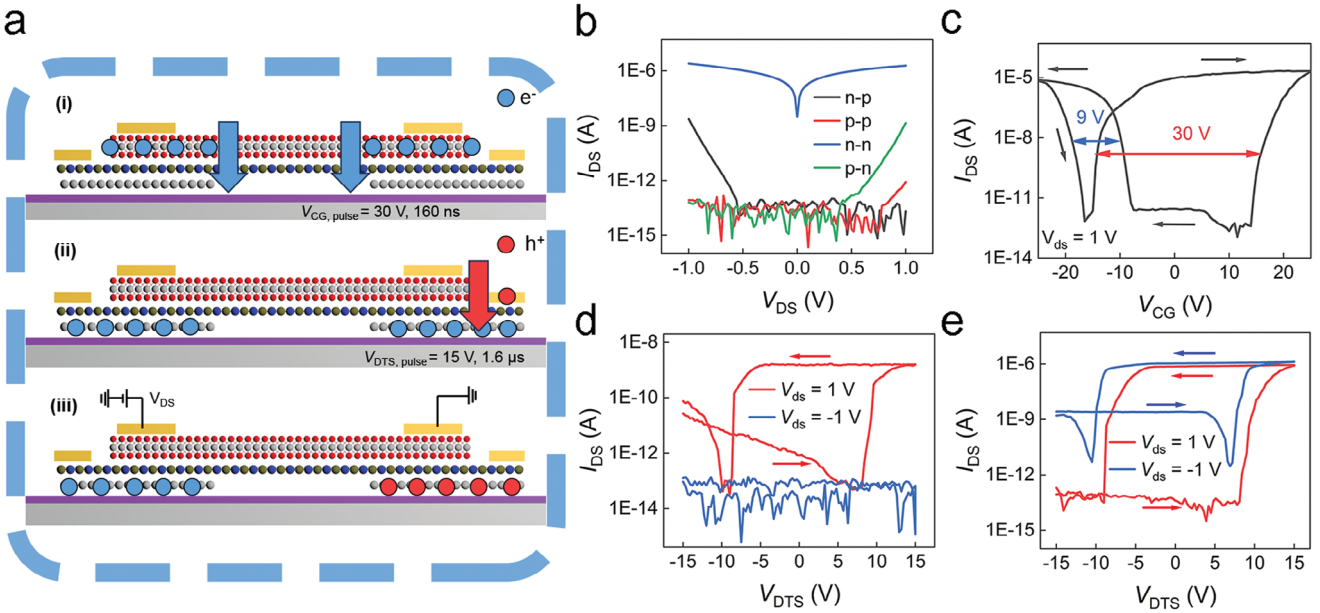



**Figure 2.** Programmable 2D $WSe_2$ lateral p-n junction controlled by dual floating gates. a) Operating principle of a lateral dual-floating-gate device. i) Electrons in the channel tunnels through hBN and be stored in the two floating gates by applying a 30 V, 160 ns pulse to the control gate. ii) Holes tunnel through hBN and neutralize the electrons in the floating gates, by applying a 15 V, 1.6 μs pulse to the DTS electrode. iii) Measurement of the channel current at $V_{DS}$ = 1 V after two floating gates storing the opposite charges. b, Output characteristics of the 2D $WSe_2$ homojunction at $V_{DS}$ = 1 V after programming. c, Transfer characteristic by dual sweeping the voltage applied to control gate at $V_{DS}$ = 1 V. d,e) Dual sweeping transfer characteristics with a forward and reverse voltage (between −15 and +15 V) scanning on the DTS electrode at $V_{DS}$ = ±1 V when the FGD stores electrons (d) or holes (e).

sequence. The thicknesses of $WSe_2$, hBN, and graphene were 4.3, 11.6, and 4.1 nm, respectively, which were measured by atomic force microscopy (AFM). The source and drain electrodes are positioned directly above the floating gates, allowing for better modulation of the Schottky barrier near metal contacts and enhancing doping capability of the floating gates on $WSe_2$.[31,49,50] The floating gate located at the drain side is referred to as FGD, while the floating gate at the source side is referred to as FGS. The electrode used to inject charges into FGD is called DTD, and the electrode used to inject charges into FGS is called DTS. The equivalent circuit diagram of the DFG-FET device is shown in the Figure 1c.

The unique performance of the device can be attributed to its structure, where the floating gates can optimize the injection of charge carriers in the contact area.[51–52] Based on the current in the $WSe_2$ transistor at $V_{CG}$ = 0 V (Figure 1d) is at the electron branch, it can be inferred that the intrinsic doping of $WSe_2$ is $n^-$-type. From Figure 1e, it can be seen that the floating gate can easily dope $WSe_2$ as n-type or p-type, with almost the same level of on-state current $I_{on} = 1 \times 10^{-6}$ A at $V_{DS}$ = 1 V. Figure 1f shows the band diagrams for different types of homojunctions under different polarities of the two floating gates and drain voltages. Figure 1g illustrates the relationship between the charge stored in the two floating gates and the conductivity of the channel. The polarity of the floating gates is determined by the polarity of the pulses injected by the two direct tunneling electrodes. When both floating gates store holes, the channel is in an n-type state, and it remains conductive regardless of the polarities of $V_{DS}$ (Figure 1f–i,ii). However, the electrons trapped in the floating gates will produce mirror-imaged charges (holes) in the $WSe_2$, which leads to the $WSe_2$ over the graphene p-doped. And the $WSe_2$ outside the floating gates remains $n^-$-type, which forms the channel a p-$n^-$-p junction, preventing current flow in both directions (Figure 1f–iii,iv). The channel will form a p-n junction (or n-p junction) as the two floating gates store opposite charges. The direction of rectification will depend on the polarity configurations of the floating gates (Figure 1f-v–viii).

Thanks to the capability of the independent control over the two floating gates, the various conductivity states mentioned above can be easily achieved. To independently inject different charges into the two floating gates, two metal electrodes were deposited on the tunneling layer above the floating gates. Therefore, the floating gates here can capture charge through two operations, which is shown in the **Figure** 2a (illustrates the operating process for forming a p-n junction). When a positive voltage pulse ($V_{CG, pulse}$ = 30 V, 160 ns) is applied to the control gate, electrons within the $WSe_2$ tunnel through hBN to reach the two floating gates via Fowler-Nordheim (FN) tunneling (Figure 2a–i). After the pulse is removed, the electrons or holes stored in the MLG will not tunnel back into the channel, but rather remain trapped within the floating gates.[53–54] When a positive pulse is applied to the direct tunneling electrode at the source (typically 15 V, 1.6 μs), holes tunnel through hBN into the MLG, neutralizing the floating gate at the source and storing holes (Figure 2a-ii). Since the two floating gates are not connected, the other side's floating gate is not affected. At this point, the two floating gates have stored different charges, resulting in the nonvolatile hole/electron doping of the two parts of the $WSe_2$ channel stacking over the two floating-gate regions and the formation of p-n junction (Figure 2a–iii). The programming speed differs

between the control gate electrode (30 V, 160 ns) and the direct tunneling electrode (15 V, 1.6 µs) due to the distinct electric field distributions generated by these electrodes. The electric field produced by the control gate (Figure S2a, Supporting Information) is uniform and equally distributed across the hBN layer. In contrast, the electric field caused by the direct tunneling electrode (Figure S2b, Supporting Information) forms between the direct tunneling electrode and the source electrode, resulting in a curved distribution. This non-uniform field often has higher electric field strengths at the edges of the electrodes. If any edge point exceeds the breakdown voltage of hBN, the tunneling layer will cease to function. Therefore, we prefer to apply a lower pulse height to the direct tunneling electrode to mitigate this risk. With a lower voltage applied to store the same amount of charge in the floating gate, a longer pulse width is required.[55]

Figure 2b shows the typical output curves across the $WSe_2$ homojunction at room temperature. When both source and drain floating gates store holes, the channel is n-n type (blue curve), and there is no rectification in both directions of the current. The currents on both sides are equal, indicating a good ohmic contact. On the contrary, if the floating gates store electrons, the channel modulated by the floating gates is p-p type (red curve). Due to the middle region showing a $n^-$-type behavior, the channel was formed a p-$n^-$-p junction preventing the current from flowing in either direction. When the two floating gates store different charges, the channel forms a p-n homojunction (green curve) or n-p homojunction (black curve), and the rectification ratios for both junctions are approximately equal at $\approx 10^5$ ($V_{DS} = \pm 1$ V).

The rectification curve of the p-n junction can be described by a modified Shockley equation:[34]

$$I_D = \frac{\eta V_T}{R_S} W\left[\frac{I_0 R_S}{\eta V_T}\exp\left(\frac{V_D + I_0 R_S}{\eta V_T}\right)\right] - I_0 \quad (1)$$

where $\eta$, $V_T$ ($V_T = k_B T/e$), $R_S$, $W$, $I_0$, $k_B$, $e$ are the ideality factor, the thermal voltage at temperature $T$, the series resistance associated with the electrode/$WSe_2$ contact, the Lambert W function, and the reverse-bias current, the Boltzmann constant, elementary electron charge, respectively. Figure S3 (Supporting Information) displays the experimental data and fitting curves of the rectification curves for $WSe_2$ n-p and p-n homojunction in a linear coordinate system. For both the p-n junction and n-p junction, the fitting results of the rectification curves match the experimental results quite well. The ideal factors for the two homojunctions are ≈1.56 and ≈1.57 respectively, showing a close approximation. This demonstrates the good symmetry of this programmable DFG-FET $WSe_2$ homojunction. The different ideal factors represent different transport mechanisms.[56] For an ideal p-n junction, an ideal factor of 1 indicates that transport is primarily diffusion-dominated, while $\eta = 2$ indicates that transport is primarily recombination-dominated. All the ideality factors extracted from p-n and n-p are approximately in the middle between 1 and 2, indicating that both diffusion and recombination mechanisms are present in this device, and they contribute to the transport behavior to a similar extent. The contribution of the recombination mechanism indicates that there is a certain amount of defect states within $WSe_2$, which act as recombination centers.[11]

Figure 2c shows the transfer characteristics of the DFG-FET device, scanning $V_{CG}$ from −25 V to 25 V and then back to −25V. The transfer curves of $WSe_2$ DFG-FET and $WSe_2$ FGFET (Floating Gate Field Effect Transistor) show distinct differences in their transfer curves, with DFG-FET exhibiting two clearly defined low-conductance plateaus. When $V_{CG}$ scans from negative to 0 V, positive charges are stored in the floating gates, modulating the channel to n-type. However, when $V_{CG} < 0$ V, the middle region is field-controlled to become p-type, forming a n-p-n junction (high-resistance state). When $V_{CG}$ scans from positive to 0 V, negative charges are stored in the floating gates, modulating the channel to p-type. However, when $V_{CG} > 0$ V, the middle region is field-controlled to become n-type, forming a p-n-p junction (high-resistance state). For the $WSe_2$ FGFET (Figure 1e), its high-resistance states pass quickly through the transfer curve without forming plateaus. To better confirm the situation of storing different charges in the two floating gates, a pulse of $V_{CG,\,pulse}$ = ±30 V, 160 ns pulse was applied to the CG to store electrons or holes on both floating gates before scanning the direct tunneling electrode on the source side. Then, another two different transfer curves were obtained by scanning the direct tunneling electrode between −15 V to +15 V once again, as presented in Figure 2d and 2e respectively. Overall, the resistive state of the device's channel is determined by the combination of $V_{CG,\,pulse}$, $V_{DT,\,pulse}$, and $V_{DS}$.

**Figure 3a** shows the retention characteristics of the $WSe_2$ device when acting as a DFG-FET memory. To better articulate how each state was achieved, (1, 1, 1) represents the $V_{CG,\,pulse} = +30$ V, 160 ns, $V_{DTD,\,pulse} = +15$ V, 1.6 µs, $V_{DS} = +1$ V. On the opposite, (0, 0, 0) represents the $V_{CG,\,pulse} = -30$ V, 160 ns, $V_{DTD,\,pulse} = -15$ V, 1.6 µs, $V_{DS} = -1$ V. Whether $V_{DS} = +1$ V nor $V_{DS} = -1$ V, the device has a pretty high on/off ratio over $10^7$. The same $WSe_2$/hBN/MLG heterojunction with double floating gates exhibits a higher rectification ratio compared to the semi-floating gate structure (Figure S4, Supporting Information). The 8 states show no significant change in current over 500 s, indicating good retention capability during this period.

The endurance performance of the DFG-FET non-volatile memory is measured by cyclic switching of the eight states in Figure 3b,c. Figure 3b shows the current state when electrons are pre-stored on FGS, followed by applying $V_{DTD,\,pulse} = \pm 15$ V, 1.6 µs, and then reading the current state within $V_{DS} = \pm 1$ V. The endurance performance in Figure 3c was tested when holes were pre-stored on FGS. The results indicate that this device can be freely switched between the eight states by applying different pulses, and the current of the eight states shows no significant decay within 250 cycles. To further improve the device's on-off ratio and rectification ratio, a high-k dielectric layer can be chosen as the tunneling layer to achieve better modulation capability and lower tunneling voltage.[11,14,20]

In integrated circuits, digital inverters are fundamental components that are crucially important. In CMOS technology, inverters are typically implemented using both NMOS and PMOS transistors. In NMOS logic, the same function can be achieved using an N-type FET and a resistor (or a depletion-mode N-type FET).[57] Figure 3d illustrates the circuit schematic of an inverter logic implemented after pre-storing holes in FGS. During the process of scanning $V_{DTD}$ from −15 to 15 V (Figure 3e), electrons are first stored in FGD followed by holes storage. The channel transitions from a p-n junction to an n-n junction and the resistance of the double floating gate memory changes

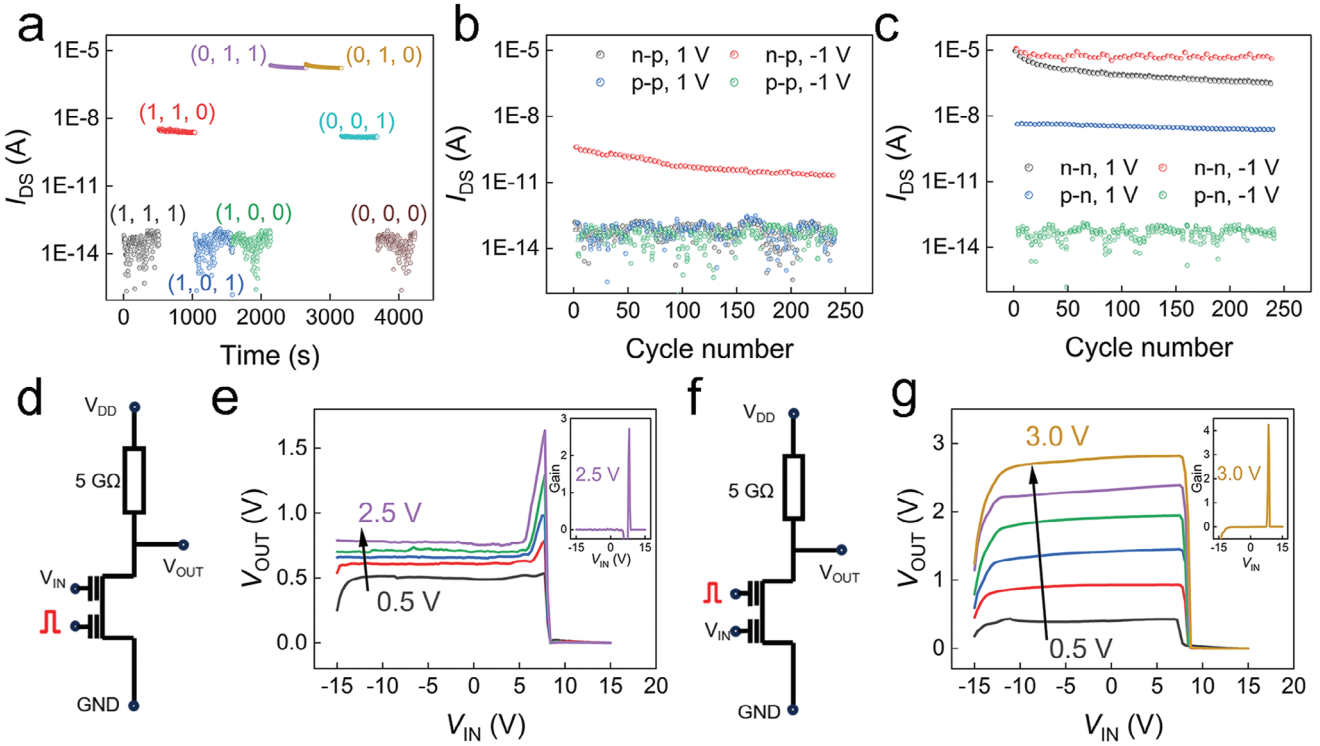



**Figure 3.** Multi-level nonvolatile memories and digital inverters based on 2D $WSe_2$ lateral homojunction. a) Retention characteristics of the non-volatile memory by recording the evolution of three current level ($I_{DS}$) over time, after adjusting the polarity of the charges within the two floating gates and reading $I_{DS}$ at $V_{DS} = \pm 1$ V at room temperature. The three numbers in parentheses represent the polarity of the pulse applied to the control gate, the polarity of the pulse applied to the DTD, and the polarity of $V_{DS}$, respectively. For example, (1, 1, 1) indicates applying a +30 V, 160 ns pulse to the control gate, then applying a +15 V, 1.6 µs pulse to DTD, and subsequently measuring $I_{DS}$ at $V_{DS} = 1$ V. b,c) Endurance characteristics of the non-volatile memory by cyclically switching the three current level, while the FGS was pre-stored electrons b) and holes c), by alternately applying $V_{DTD,\ pulses} = \pm 15$ V, 1.6 µs and reading $I_{DS}$ at $V_{DS} = \pm 1$ V. d,f) Circuit diagram of the inverter based on a $WSe_2$ homojunction, in which the FGS (or FGD) was storing holes, the source electrode is grounded, drain and DTD (or DTS) electrodes are connected to the output and input terminals, respectively, $V_{DD}$ is connected with a 5 GΩ resistor to drive the device. e) Output curves of the inverter with DTD as the input at various $V_{DD}$ ($V_{DD} = 0.5$ V for black curve and then increases from 0.5 to 2.5 V in a step of 0.5 V). The inset shows the voltage gain under $V_{DD} = 2.5$ V. g) Output curves of the inverter with DTS as the input at various $V_{DD}$ ($V_{DD} = 0.5$ V for black curve and then changes from 0.5 to 3 V in a step of 0.5 V). The inset shows the voltage gain under $V_{DD} = 3.0$ V.

from ≈$10^9$ to ≈$10^6$ Ω. Figure 3f depicts the circuit schematic of an inverter configured after pre-storing holes in FGD. During the $V_{DTS}$ scanning process from −15 to 15 V (Figure 3g), the FGS initially stores electrons followed by holes injection. This results in a transition of the channel from an n-p junction to an n-n junction, accompanied by an increase in the resistance of the double floating gate memory from ≈$10^{13}$ to ≈$10^6$ Ω. As $V_{DD}$ increases, the gain of the inverter also increases (Figure S5, Supporting Information). At $V_{DD} = 2.5$ V, the gain of the inverter configured in Figure 3e is 2.7. At $V_{DD} = 3.0$ V, the gain of the inverter configured in Figure 3g is 4.3.

The p-n junction can serve as a photovoltaic device, as the photo-excited charge carriers under light irradiation can separate under the built-in electric field to form a voltage difference. **Figure** 4a presents the schematic diagram of the $WSe_2$ homojunction under 633 nm laser irradiation. Figure 4b shows the $I_{DS}$-$V_{DS}$ curves at $V_{DS}$ ranging from −1 to 1 V of the $WSe_2$ double floating gate homojunction forming a p-n junction (bottom) and an n-p junction (top) in the dark and under light illumination of a 633 nm, 5.63 nW laser. The black curve in the dark condition shows obvious rectification behavior. Under the 5.63 nW laser illumination, the p-n junction produces an obvious photocurrent, showing a positive open-circuit voltage ($V_{OC}$) and a negative short-circuit current ($I_{SC}$). Both homojunction exhibit nearly identical photo-current responses under the same power and wavelength laser illumination, indicating good device symmetry. For the n-n junction (Figure S6b, Supporting Information), there is no significant difference in current between darkness and laser irradiation. For the p-p junction (Figure S6a, Supporting Information), however, it exhibits a different behavior. It shows the same large photocurrent at $V_{DS} = 1$ V and $V_{DS} = -1$ V, symmetrically, but does not exhibit the photovoltaic effect. This indicates that the photovoltaic and photoelectric effects can only be realized for the $WSe_2$ p-n and n-p homojunction. With the increase in laser power from 0.09 to 180 nW, $V_{OC}$ and $I_{SC}$ of the $I_{DS}$-$V_{DS}$ curve gradually increases, which is shown in Figure 4c, indicating the device's capability for photovoltaic energy conversion. Figure 4d shows the dynamic performance of the $WSe_2$ p-n junction and n-p junction under cyclic operation with darkness and 5.63 nW laser irradiation. It can be observed that the photocurrent quickly responds to low-power laser irradiation. The directions of the photocurrent in the p-n junction and n-p

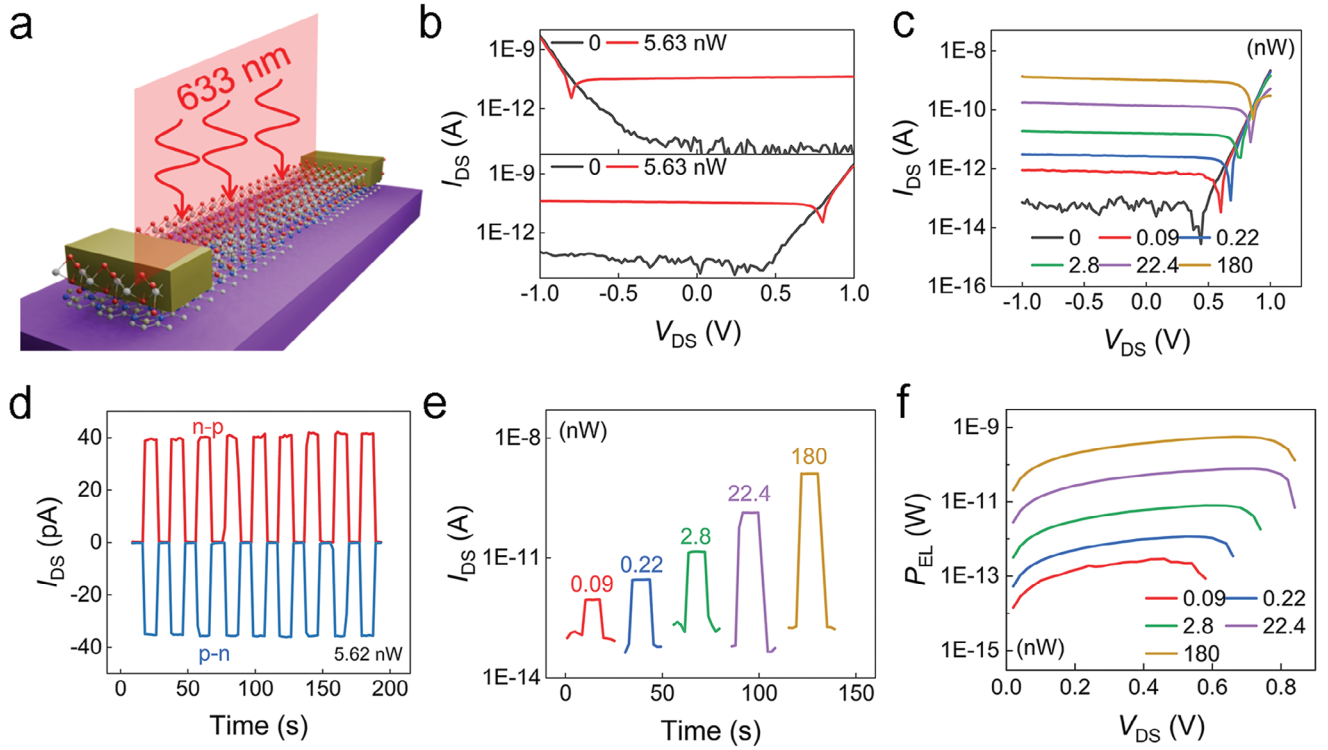



**Figure 4.** Photovoltaic and optoelectronic characteristics of $WSe_2$ p-n and n-p junctions. a) Schematic diagram of a $WSe_2$ homojunction device under 633 nm laser illumination. b) Output curves of $WSe_2$ n-p (upper panel) and p-n (lower panel) junctions in the dark (black) and under 633 nm laser illumination with a power of 5.62 nW (red). c) $I_{DS}$-$V_{DS}$ output curves of the 2D $WSe_2$ p-n homojunction in the dark and under light illumination by a 633 nm laser with different power levels. The laser power increases from 0 (black) to 0.09 (red), 0.22 (blue), 2.8 (green), 22.4 (violet), and 180 (khaki) nW. d) Time-dependent short-circuit photocurrent for $WSe_2$ n-p (red) and p-n (blue) junctions in the dark and under 5.62 nW 633 nm laser illumination at $V_{DS}$ = 0 V, indicating that the $WSe_2$ p-n and n-p junction shows an apparent and robust photoelectrical response. e) photocurrent of the $WSe_2$ p-n junction under illumination by a 633 nm laser with increasing power levels at $V_{DS}$ = 0 V. f) Output electrical power ($P_{EL}$) as a function of $V_{DS}$ under different laser powers.

junction are opposite because of the opposite directions of the built-in electric fields. The photocurrent in the p-n junction is back forward at $V_{DS}$ = 0 V, while the photocurrent in the n-p junction is forward. This ability for fast detection under weak light can be further developed into photonic devices, photovoltaic devices, and optoelectronic logic devices. Figure 4e shows the photocurrent of the $WSe_2$ p-n homojunction as it varies with laser power from 0.09 to 180 nW. A clear photocurrent switching behavior can be observed. The electrical power ($P_{EL}$) is plotted in Figure 4f, which can be calculated by $P_{EL} = I_{DS} \times V_{DS}$. The maximum output electrical power ($P_{EL,\,max}$) varies from $V_{DS}$ = 0.60 to 0.86 V, which implies that the optimal output working voltage for these devices, when utilized in photovoltaic cells to achieve maximum energy conversion, is ≈0.7 V. The fill factor (FF = $P_{EL,\,max}/I_{SC} \times V_{OC}$), electrical power conversion efficiency ($\eta_{EPCE} = P_{EL,\,max}/P_{laser}$), photovoltage responsivity ($V_{OC}/P_{laser}$), and open-circuit voltage can also be extracted, as shown in **Figure 5a**. The power conversion efficiency can reach 0.53%. By selecting an appropriate thickness, the transparency of the material can be balanced with the efficiency of photoelectric conversion.[11] As shown in Figure 5b, $I_{SC}$ and $P_{laser}$ exhibit the following exponential relationship:

$$I_{SC} \propto P_{laser}^{\alpha} \tag{2}$$

with a fitted exponent $\alpha = 0.96$. Within the range of laser power used in the experiment, no saturation of the short-circuit current is observed, suggesting the presence of sufficient defect states in the $WSe_2$ material. The external quantum efficiency (EQE) represents the ratio of collected charge carriers to the number of incident photons:

$$I_{SC} = P_{laser} \times EQE \times \lambda e/hc \tag{3}$$

where $\lambda$, $e$, $h$, and $c$ are the wavelength of the incident light, electron charge, Planck's constant, and speed of light, respectively.[56] The peak EQE in this device is 2.4%, as illustrated in Figure 5c. The photoelectric performance of our devices, in comparison with other $WSe_2$ p-n junction devices, is detailed in Table S1 (Supporting Information).

For the steady-state open-circuit condition, the carrier concentration of the p-n junction is determined by the balance between the photo-generated carriers and the interlayer recombination carriers. The resulting open-circuit voltage ($V_{OC}$) can be described by the following formula:

$$\frac{dV_{OC}}{dln\left(P_{laser}\right)} = \frac{2}{\beta}\frac{k_B T}{e} \tag{4}$$

a

| laser power (nW) | $V_{OC}$ (V) | $I_{SC}$ (A) | $P_{EL,\ MAX}$ (W) | Fill factor | Efficiency (%) | Responsivity ($10^9$V/W) |
|---|---|---|---|---|---|---|
| 0.09 | 0.60 | $7.41\times10^{-13}$ | $2.91\times10^{-13}$ | 0.65 | 0.32 | 6.67 |
| 0.22 | 0.68 | $2.70\times10^{-12}$ | $1.16\times10^{-12}$ | 0.63 | 0.53 | 3.09 |
| 2.8 | 0.76 | $1.58\times10^{-11}$ | $7.99\times10^{-12}$ | 0.67 | 0.29 | 0.27 |
| 22.4 | 0.84 | $1.41\times10^{-10}$ | $7.76\times10^{-11}$ | 0.65 | 0.35 | 0.04 |
| 180 | 0.86 | $1.03\times10^{-9}$ | $5.58\times10^{-10}$ | 0.63 | 0.31 | 0.005 |

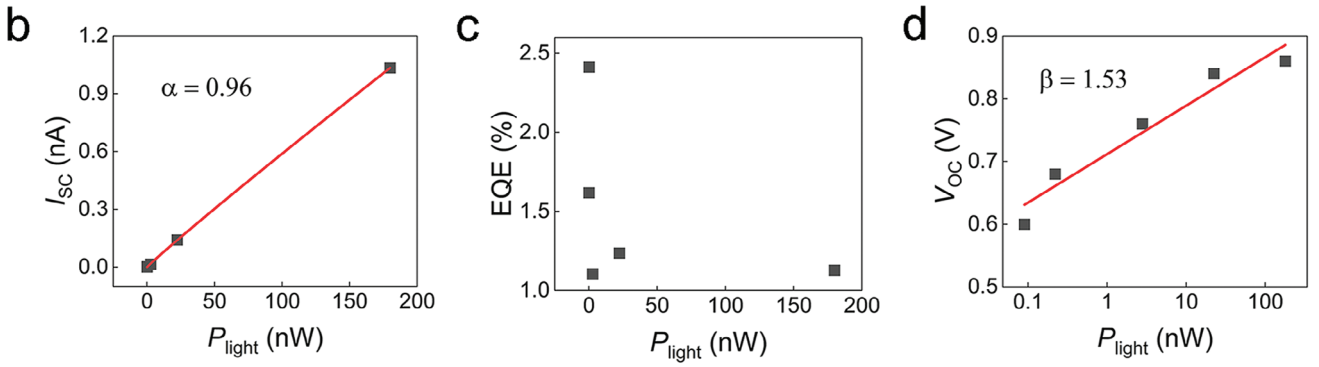



**Figure 5.** Short-circuit current ($I_{SC}$) and open-circuit voltage ($V_{OC}$) as a function of incident laser power ($P_{laser}$) for the $WSe_2$ p-n homojunction. a) Summary of the optoelectronic properties of the $WSe_2$ homojunction under different laser powers, including open-circuit voltage ($V_{OC}$), short-circuit current ($I_{SC}$), maximum output electrical power ($P_{EL,\ MAX}$), fill factor (FF), electrical power conversion efficiency ($\eta_{EPCE}$), and responsivity. b) $I_{SC}$ as a function of $P_{laser}$, showing a power-law relationship of $I_{SC} \propto P_{laser}{}^{\alpha}$ with $\alpha = 0.96$. c) $P_{laser}$-dependent EQE extracted by fitting the $I_{SC}$-$P_{laser}$ curve in (b). d) $V_{OC}$ as a function of $P_{laser}$ on a logarithmic scale, where $\beta = 1.53$ is extracted from the linear fitting curve.

where $T$ is the absolute temperature and $\beta$ is the recombination order. When $\beta = 1$, the recombination process is mainly governed by monomolecular (Shockley-Read-Hall, SRH) recombination, but when $\beta = 2$, it is mainly governed by bimolecular (Langevin) recombination.[58] The fitting from the experimental results in Figure 5d yields $\beta = 1.53$. This indicates that both recombination processes, SRH and Langevin, are at play in the device, suggesting that $WSe_2$ material still contains a certain amount of defect states. The device's photovoltaic response ($V_{OC}/P_{laser}$) reaches $6.67 \times 10^9$ V $W^{-1}$ at a laser power of 0.09 nW, indicating that the device qualifies as an ultra-sensitive photodetector. This double-gate storage device can serve as a more flexible optoelectronic memory, capable of storing and converting photoelectric information, and allowing for easy adjustment of the device configuration.

## 3. Conclusion

In conclusion, a novel non-volatile programmable $WSe_2$ 2D lateral p-n junction, based on van der Waals heterostructures, has been successfully fabricated employing a dual-floating-gate device architecture. By injecting charges into the two floating gates, it is possible to achieve four different doping configurations of the homojunction: p-n, n-p, n-n and p-p. The $WSe_2$ p-n and n-p junctions exhibit nonvolatile and reconfigurable characteristics, with a rectification ratio close to $10^5$ and similar ideal factors of ≈1.56 and 1.57. Additionally, the $WSe_2$ p-n and n-p junctions demonstrate highly sensitive photoelectric and photovoltaic responses to low-power 633 nm laser illumination. When the laser power is 0.22 nW, the photoelectric conversion efficiency is 0.53%, and when the optical power is 0.09 nW, the photovoltaic response is $6.67 \times 10^9$ V $W^{-1}$. This new type of lateral dual-gate structure provides a new development direction for future electronic and optoelectronic devices.

## 4. Experimental Section

*Fabrication of the Device*: The $WSe_2$, hBN, and graphite bulk crystals were purchased from 2D Semiconductors, HQ Graphene, and NGS Naturgraphit, respectively. The silicon chip with 285 nm silicon dioxide was first treated with oxygen plasma. Then the multi-layer graphene was dry transferred using 3 M Scotch tape, annealed at 400 degrees Celsius in a vacuum furnace with 10% $H_2$/Ar atmosphere for 200 min. Then, the few-layer graphene was patterned by electron-beam lithography and treated with oxygen plasma. With the aid of a transfer stage under an optical microscope, the mechanically exfoliated hBN, $WSe_2$ on PDMS were aligned and transferred onto the graphene floating gates inside a glovebox with $O_2$ and $H_2O$ concentrations below 0.1 ppm. The 5/50 nm Cr/Au metal electrodes were fabricated using regular EBL, EBD, and lift-off processes. Atomic force microscopy (AFM, Asylum Research, Cypher S) was used under ambient conditions in tapping mode to measure the thicknesses of $WSe_2$, hBN, and MLG flakes. The fabrication process scheme is illustrated in Figure S1 (Supporting Information).

*Electrical Characterization of the Device*: The electrical properties of the devices were probed with a Keithley 4200 semi-conductor characterization system (4200-SCS) in a Lake Shore vacuum chamber (~$10^{-4}$ Pa) at room temperature. The voltage pulses with FWHM of 160 ns were performed in the 4200-SCS system equipped with 4225-PMU and 4225-RPM units. The

devices were illuminated with a 633 nm wavelength laser, and an attenuator was used to adjust its power. The laser intensity was measured using an optical power meter.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

This work was supported by the National Key Research & Development Projects of China (Grant No. 2022YFA1204100), National Natural Science Foundation of China (Grant Nos. 62488201), CAS Project for Young Scientists in Basic Research (YSBR-003), the Innovation Program of Quantum Science and Technology (2021ZD0302700).

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

floating gate, photovoltaic, p-n homojunction, rectification, van der Waals heterostructures

Received: November 27, 2024
Revised: January 23, 2025
Published online:

[1] D. Lembke, S. Bertolazzi, A. Kis, *Acc. Chem. Res.* **2015**, *48*, 100.
[2] Q. Cheng, J. Pang, D. Sun, J. Wang, S. Zhang, F. Liu, Y. Chen, R. Yang, N. Liang, X. Lu, Y. Ji, J. Wang, C. Zhang, Y. Sang, H. Liu, W. Zhou, *InfoMat.* **2020**, *2*, 656.
[3] Q. H. Wang, K. Kalantar-Zadeh, A. Kis, J. N. Coleman, M. S. Strano, *Nat. Nanotechnol.* **2012**, *7*, 699.
[4] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **2011**, *6*, 147.
[5] M. S. Fuhrer, J. Hone, *Nat. Nanotechnol.* **2013**, *8*, 146.
[6] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, A. Javey, *Nano Lett.* **2012**, *12*, 3788.
[7] S. Larentis, B. Fallahazad, E. Tutuc, *Appl. Phys. Lett.* **2012**, *101*, 223104.
[8] Y.-F. Lin, Y. Xu, S.-T. Wang, S.-L. Li, M. Yamamoto, A. Aparecido-Ferreira, W. Li, H. Sun, S. Nakaharai, W.-B. Jian, K. Ueno, K. Tsukagoshi, *Adv. Mater.* **2014**, *26*, 3263.
[9] O. Lopez-Sanchez, D. Lembke, M. Kayci, A. Radenovic, A. Kis, *Nat. Nanotechnol.* **2013**, *8*, 497.
[10] L. Britnell, R. M. Ribeiro, A. Eckmann, R. Jalil, B. D. Belle, A. Mishchenko, Y.-J. Kim, R. V. Gorbachev, T. Georgiou, S. V. Morozov, A. N. Grigorenko, A. K. Geim, C. Casiraghi, A. H. C. Neto, K. S. Novoselov, *Science.* **2013**, *340*, 1311.
[11] A. Pospischil, M. M. Furchi, T. Mueller, *Nat. Nanotechnol.* **2014**, *9*, 257.
[12] C.-H. Lee, G.-H. Lee, A. M. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, P. Kim, *Nat. Nanotechnol.* **2014**, *9*, 676.
[13] R. S. Sundaram, M. Engel, A. Lombardo, R. Krupke, A. C. Ferrari, P. Avouris, M. Steiner, *Nano Lett.* **2013**, *13*, 1416.
[14] J. S. Ross, P. Klement, A. M. Jones, N. J. Ghimire, J. Yan, D. G. Mandrus, T. Taniguchi, K. Watanabe, K. Kitamura, W. Yao, D. H. Cobden, X. Xu, *Nat. Nanotechnol.* **2014**, *9*, 268.
[15] R. Cheng, D. Li, H. Zhou, C. Wang, A. Yin, S. Jiang, Y. Liu, Y. Chen, Y. Huang, X. Duan, *Nano Lett.* **2014**, *14*, 5590.
[16] F. Wu, H. Tian, Y. Shen, Z. Hou, J. Ren, G. Gou, Y. Sun, Y. Yang, T.-L. Ren, *Nature.* **2022**, *603*, 259.
[17] J. Jiang, M.-H. Doan, L. Sun, H. Kim, H. Yu, M.-K. Joo, S. H. Park, H. Yang, D. L. Duong, Y. H. Lee, *Adv. Sci.* **2020**, *7*, 1902964.
[18] D. Akinwande, C. Huyghebaert, C.-H. Wang, M. I. Serna, S. Goossens, L.-J. Li, H. S. P. Wong, F. H. L. Koppens, *Nature.* **2019**, *573*, 507.
[19] D. Wang, X.-B. Li, H.-B. Sun, *Nano Lett.* **2021**, *21*, 6298.
[20] B. W. H. Baugher, H. O. H. Churchill, Y. Yang, P. Jarillo-Herrero, *Nat. Nanotechnol.* **2014**, *9*, 262.
[21] D. J. Groenendijk, M. Buscema, G. A. Steele, S. Michaelis de Vasconcellos, R. Bratschitsch, H. S. J. van der Zant, A. Castellanos-Gomez, *Nano Lett.* **2014**, *14*, 5846.
[22] M. Buscema, D. J. Groenendijk, G. A. Steele, H. S. J. van der Zant, A. Castellanos-Gomez, *Nat. Commun.* **2014**, *5*, 4651.
[23] N. M. Gabor, J. C. W. Song, Q. Ma, N. L. Nair, T. Taychatanapat, K. Watanabe, T. Taniguchi, L. S. Levitov, P. Jarillo-Herrero, *Science.* **2011**, *334*, 648.
[24] C. Pan, C.-Y. Wang, S.-J. Liang, Y. Wang, T. Cao, P. Wang, C. Wang, S. Wang, B. Cheng, A. Gao, E. Liu, K. Watanabe, T. Taniguchi, F. Miao, *Nat. Electron.* **2020**, *3*, 383.
[25] C. Tan, H. Wang, X. Zhu, W. Gao, H. Li, J. Chen, G. Li, L. Chen, J. Xu, X. Hu, L. Li, T. Zhai, *ACS Appl. Mater. Interfaces.* **2020**, *12*, 44934.
[26] Z.-Q. Xu, Y. Zhang, Z. Wang, Y. Shen, W. Huang, X. Xia, W. Yu, Y. Xue, L. Sun, C. Zheng, Y. Lu, L. Liao, Q. Bao, *2D Mater.* **2016**, *3*, 041001.
[27] A. Tavkhelidze, L. Jangidze, Z. Taliashvili, N. E. Gorji, *Coatings.* **2021**, *11*, 945.
[28] A. Tavkhelidze, L. Jangidze, G. Skhiladze, S. Sikharulidze, K. Dzneladze, R. Kvesitadze, A. Bibilashvili, *Nanomaterials.* **2024**, *14*, 1889.
[29] A. Tavkhelidze, *Phys. E:Low-Dimens. Syst. Nanostruct.* **2014**, *60*, 4.
[30] G. Wu, B. Tian, L. Liu, W. Lv, S. Wu, X. Wang, Y. Chen, J. Li, Z. Wang, S. Wu, H. Shen, T. Lin, P. Zhou, Q. Liu, C. Duan, S. Zhang, X. Meng, S. Wu, W. Hu, X. Wang, J. Chu, J. Wang, *Nat. Electron.* **2020**, *3*, 43.
[31] L. Lv, F. Zhuge, F. Xie, X. Xiong, Q. Zhang, N. Zhang, Y. Huang, T. Zhai, *Nat. Commun.* **2019**, *10*, 3331.
[32] G. Wu, X. Wang, Y. Chen, S. Wu, B. Wu, Y. Jiang, H. Shen, T. Lin, Q. Liu, X. Wang, P. Zhou, S. Zhang, W. Hu, X. Meng, J. Chu, J. Wang, *Adv. Mater.* **2020**, *32*, 1907937.
[33] Y. Zhao, M. Chi, J. Liu, J. Zhai, *Discover Nano.* **2023**, *18*, 83.
[34] D. Li, M. Chen, Z. Sun, P. Yu, Z. Liu, P. M. Ajayan, Z. Zhang, *Nat. Nanotechnol.* **2017**, *12*, 901.
[35] H. Wang, L. Bao, R. Guzman, K. Wu, A. Wang, L. Liu, L. Wu, J. Chen, Q. Huan, W. Zhou, S. T. Pantelides, H.-J. Gao, *Adv. Mater.* **2023**, *35*, 2301067.
[36] R. Cheng, L. Yin, F. Wang, Z. Wang, J. Wang, Y. Wen, W. Huang, M. G. Sendeku, L. Feng, Y. Liu, J. He, *Adv. Mater.* **2019**, *31*, 1901144.
[37] T. Jin, J. Gao, Y. Wang, Y. Zheng, S. Sun, L. Liu, M. Lin, W. Chen, *Nano Res.* **2022**, *15*, 4439.
[38] S. Wang, G. Geng, Y. Sun, S. Wu, X. Hu, E. Wu, J. Liu, *Nano Res.* **2022**, *15*, 6507.

[39] Y. Tang, Z. Wang, P. Wang, F. Wu, Y. Wang, Y. Chen, H. Wang, M. Peng, C. Shan, Z. Zhu, S. Qin, W. Hu, *Small.* **2019**, *15*, 1805545.
[40] S. Ko, J. Na, Y.-S. Moon, U. Zschieschang, R. Acharya, H. Klauk, G.-T. Kim, M. Burghard, K. Kern, *ACS Appl. Mater. Interfaces.* **2017**, *9*, 42912.
[41] Y. Yang, N. Huo, J. Li, *J. Mater. Chem. C.* **2018**, *6*, 11673.
[42] J. Sun, Y. Wang, S. Guo, B. Wan, L. Dong, Y. Gu, C. Song, C. Pan, Q. Zhang, L. Gu, F. Pan, J. Zhang, *Adv. Mater.* **2020**, *32*, 1906499.
[43] F. Lu, J. Gao, H. Yang, Q. Zhao, J. Deng, X. Liu, W. Wang, S. Fan, *Phys. E: Low-Dimens. Syst. Nanostruct.* **2024**, *158*, 115907.
[44] Z. Sheng, J. Dong, W. Hu, Y. Wang, H. Sun, D. W. Zhang, P. Zhou, Z. Zhang, *Nano Lett.* **2023**, *23*, 5242.
[45] J.-W. Chen, S.-T. Lo, S.-C. Ho, S.-S. Wong, T.-H.-Y. Vu, X.-Q. Zhang, Y.-D. Liu, Y.-Y. Chiou, Y.-X. Chen, J.-C. Yang, Y.-C. Chen, Y.-H. Chu, Y.-H. Lee, C.-J. Chung, T.-M. Chen, C.-H. Chen, C.-L. Wu, *Nat. Commun.* **2018**, *9*, 3143.
[46] A. K. Tagantsev, I. Stolichnov, E. L. Colla, N. Setter, *J. Appl. Phys.* **2001**, *90*, 1387.
[47] A. Kumar, P. K. Ahluwalia, *Eur. Phys. J. B.* **2012**, *85*, 186.
[48] H. Terrones, F. López-Urías, M. Terrones, *Sci. Rep.* **2013**, *3*, 1549.
[49] C. Kim, I. Moon, D. Lee, M. S. Choi, F. Ahmed, S. Nam, Y. Cho, H.-J. Shin, S. Park, W. J. Yoo, *ACS Nano.* **2017**, *11*, 1588.
[50] A. Rajapitamahuni, J. Hoffman, C. H. Ahn, X. Hong, *Nano Lett.* **2013**, *13*, 4374.
[51] J. Yi, X. Sun, C. Zhu, S. Li, Y. Liu, X. Zhu, W. You, D. Liang, Q. Shuai, Y. Wu, D. Li, A. Pan, *Adv. Mater.* **2021**, *33*, 2101036.
[52] X. Sun, C. Zhu, H. Liu, B. Zheng, Y. Liu, J. Yi, L. Fang, Y. Liu, X. Wang, M. Zubair, X. Zhu, X. Wang, D. Li, A. Pan, *Sci. Bull.* **2020**, *65*, 2007.
[53] L. Wu, A. Wang, J. Shi, J. Yan, Z. Zhou, C. Bian, J. Ma, R. Ma, H. Liu, J. Chen, Y. Huang, W. Zhou, L. Bao, M. Ouyang, S. J. Pennycook, S. T. Pantelides, H.-J. Gao, *Nat. Nanotechnol.* **2021**, *16*, 882.
[54] L. Liu, C. Liu, L. Jiang, J. Li, Y. Ding, S. Wang, Y.-G. Jiang, Y.-B. Sun, J. Wang, S. Chen, D. W. Zhang, P. Zhou, *Nat. Nanotechnol.* **2021**, *16*, 874.
[55] X. Sun, C. Zhu, J. Yi, L. Xiang, C. Ma, H. Liu, B. Zheng, Y. Liu, W. You, W. Zhang, D. Liang, Q. Shuai, X. Zhu, H. Duan, L. Liao, Y. Liu, D. Li, A. Pan, *Nat. Electron.* **2022**, *5*, 752.
[56] H. Wang, K. Wu, H. Guo, H. Gao, L. Liu, L. Wu, J. Chen, H. Yang, L. Bao, H.-J. Gao, *2D Mater.* **2023**, *10*, 035019.
[57] L. Wu, J. Shi, Z. Zhou, J. Yan, A. Wang, C. Bian, J. Ma, R. Ma, H. Liu, J. Chen, Y. Huang, W. Zhou, L. Bao, M. Ouyang, S. T. Pantelides, H.-J. Gao, *Nano Res.* **2020**, *13*, 1127.
[58] M. M. Furchi, A. Pospischil, F. Libisch, J. Burgdörfer, T. Mueller, *Nano Lett.* **2014**, *14*, 4785.